



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/775,448

02/10/2004

James R. Goodman

960296.00019

9410

23598

7590

06/30/2006

BOYLE FREDRICKSON NEWHOLM STEIN & GRATZ, S.C.
250 E. WISCONSIN AVENUE
SUITE 1030
MILWAUKEE, WI 53202

EXAMINER

VO, THANH DUC

ART UNIT

PAPER NUMBER

2189

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/775,448

Applicant(s)

GOODMAN ET AL.

Examiner

Thanh D. Vo

Art Unit

2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2006.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-23 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 21 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on June 12, 2006. Claims 1-2, 4, 6-7, 9, 12-13, 17-19, and 21-22 have been amended. Claims 1-23 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-23 are rejected under 35 U.S.C. 102(a) or 35 U.S.C. 102(b) as being anticipated by Rajwar (Thesis title: Speculation-based Techniques for Transactional Lock-free Execution of Lock-based Programs).

Claims 1-23 are rejected under 35 U.S.C. 102(a) since the inventive entity of the dissertation is different than the inventive entity of the current application in addition to the assumption that dissertation was first available to the public on April 25, 2003 as asserted by the Applicant on page 9 of the Remarks.

Claims 1-23 stand rejected under 35 U.S.C 102(b) with the assumption that the thesis was available to the public one year before the filing date of the current application in addition to the 37 CFR 1.105 Requirement for Information attached in this Office Action.

As per claim 1, Rajwar discloses a processor unit for a shared-memory computer comprising:

a processor (Chapter 2, page 13, line 25, wherein the author introduces a multiprocessing system);

a local memory system executing a protocol to share data with at least one other processor unit (Chapter 2, page 13, section 2.1, lines 25-30);

a conflicts resolution circuit executing a hardware program to:

(i) detect a critical section in an executing program and begin speculative execution of the critical section without acquisition of a lock (Chapter 3, page 51, Fig. 3-5, and second sentence; wherein the author disclosed a speculative lock-free execution of a critical section);

(ii) in the event of a conflict with another processor unit executing the critical section and needing to write to data within the critical section, establishing a priority between the processor units to resolve the conflict without acquisition of the lock (Chapter 4, page 100, lines 28-30).

As per claim 2, Rajwar discloses a processor unit further including:
a globally unique clock (Section 4.3.1.2, page 102, lines 27-32); and
where the conflicts resolution circuit establishes a priority between the processor units by:

- (a) time stamping requests for data sent by a given processor unit to other processor units with a value of the globally unique clock (Section 4.3.1.2, page 102);
- (b) releasing owned data requested by a second processor unit making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the second processor unit (Section 4.3.1.2, first paragraph; wherein the owned data is released to an earlier time stamp); and
- (c) deferring release of owned data requested by the second processor unit making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the second processor unit (page 106, last paragraph).

As per claim 3, Rajwar discloses a processor wherein the conflicts resolution circuit executes hardware program step (i) only during execution of a critical section (See page 9, second paragraph).

As per claim 4, Rajwar discloses a processor unit wherein the conflicts resolution circuit defers to the protocol of the local memory during execution of a section of the program. See page 8, item 2 of Transactional Lock Removal.

As per claim 5, Rajwar discloses a processor unit wherein the protocol of the local memory is a cache coherence protocol. See Section 2.1.2 Cache coherence protocols, page 17, lines 1-10.

As per claim 6, Rajwar discloses a processor unit wherein the globally unique clock includes a time variant field and a static processor-unit-dependant field. See Section 4.3.1.2, page 102, lines 24-32 regarding logical clock and processor ID.

As per claim 7, Rajwar discloses a processor unit wherein the globally unique clock is a counter updated after executions by the processor of a critical section of a program subject to a lock. See page 8, line 30 – page 9, line 3, wherein the timestamp is being updated.

As per claim 8, Rajwar discloses a processor unit wherein the counter sets itself to a higher number on updating. See page 103, first paragraph.

As per claim 9, Rajwar discloses a processor unit wherein the counter sets itself to the time stamp of the request of the second processor unit when the release of data is deferred because the time stamp of the request of the second processor unit is later. See page 104, Lamport's logical clocks.

As per claim 10, Rajwar discloses a processor unit further including buffer memory storing the deferred request of the other processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a time after the deferring to release data to the other processor unit. See Section 2.4.2 Handling speculative state, lines 20-32; Fig. 4-6; and Section 4.4.2.

As per claim 11, Rajwar discloses a processor unit further including:

a critical section detection circuit detecting the start and end of execution by the processor of a critical section of a program subject to a lock (See Section 3.9.1.1, page 63, lines 12-20); and

wherein the later time is the completion of a critical section. See Section 3.9.1.1, page 64, lines 24-20.

As per claim 12, Rajwar discloses a processor unit wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to a second processor unit when the request by the second processor unit is deferred based on its time stamp. See Section 4.4.2.2, page 118, lines 13-20.

As per claim 13, Rajwar discloses a processor unit wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a marker message to a second processor unit when the request by the second processor unit is deferred because the requested data is not available. See Section 4.4.2.2, page 118, lines 12-16.

As per claim 14, Rajwar discloses a processor wherein the conflicts resolution circuit further executes the hardware program to:

(iv) send a probe message to a third processor unit containing a time stamp of the request of a second processor unit receiving the marker message. See Section 4.4.2.2, page 119, lines 15-20.

As per claim 15, Rajwar discloses a processor wherein the conflicts resolution circuit further executes the hardware program to:

(iv) respond to a probe message to a second processor unit that has sent the processor unit a marker message indicating that a request by the processor unit has been deferred, the probe message indicating a time stamp of a third processor unit earlier than the time stamp of the request used by processor unit to acquire that data, the probe message being from a third processor unit requesting the data from the second processor unit. See pages 119, lines 20-29; page 120, lines 1-20.

As per claim 16, Rajwar discloses a processor unit further including:
a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock (See 3.9.1.1 and page 51, lines 26-30);

(ii) speculatively execute the critical section without acquiring the lock (Chapter 3, page 51, lines 27-29, and Fig. 3-5);

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit (Chapter 4, pages 100, lines 25-30, and page 101, lines 1-4); and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section. See page 94, first paragraph.

As per claim 18, Rajwar discloses a processor unit wherein the conflict resolution circuit causes a ceasing of the speculative execution of the critical section when the conflict is resolved by releasing the data per hardware program step (iii). See Section 3.2, page 48, lines 15-25.

As per claim 19, Rajwar discloses a processor unit further including buffer memory storing deferred requests from the another processor unit; and

wherein the conflicts resolution circuit further executes the hardware program to:

(iv) read the buffered deferred requests at a later time to release data to the another processor unit (see Section 4.4.2.2, lines 6-20); and

(v) cease the speculative execution of the critical section when buffer memory is exhausted. See Section 3.9.4.3 Resource-constraint of page 74.

As per claim 20, Rajwar further discloses a processor unit including buffer memory storing the results of speculative execution; and

wherein the lock elision circuit further executes the hardware program to:

(iv) cease the speculative execution of the critical section when buffer memory is exhausted. See Section 3.9.4.3 Resource-constraint of page 74.

As per claim 21, Rajwar discloses a processor unit system comprising a plurality of processor units having:

a processor (Chapter 2, page 13, wherein the author introduces a multiprocessing system);

a local memory system executing a protocol to share data with at least one other processor unit (Chapter 2, page 13, section 2.1);

a globally unique clock (Section 4.3.1.2, page 102, lines 29-32);

a conflicts resolution circuit executing a hardware program to:

(i) time stamp requests for data sent by a given processor unit to other processor units with a value of the globally unique clock (Section 4.3.1.2, page 102);

(ii) release owned data requested by a second processor unit making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the

data by the second processor unit (see Section 4.3.1.2, page, 102, first paragraph; wherein the owned data is released to an earlier time stamp); and

(iii) defer release of owned data requested by the second processor unit making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the second processor unit. See page 119, lines 14-28, last paragraph.

As per claim 22, Rajwar discloses a method of operating a set of processor units for a shared-memory computer comprising the steps of:

(a) generating on each processor unit a globally unique clock (Section 4.3.1.2, page 102, lines 29-32);

(b) time stamping all requests for data sent by a given processor unit to other processor units with a value of the globally unique clock (Section 4.3.1.2, page 102);

(c) releasing owned data requested by a second processor unit making a request with an earlier time stamp than a time stamp of a request to acquire ownership of the data by the second processor unit (Section 4.3.1.2, page 102 first paragraph; wherein the owned data is released to an earlier time stamp); and

(d) deferring release of owned data requested by the second processor unit making a request having a later time stamp than the time stamp of the request to acquire ownership of the data by the second processor unit. See page 119, lines 14-28, last paragraph.

As per claim 23, Rajwar discloses a processor unit for a shared-memory computer comprising:

a processor (Chapter 2, page 13, wherein the author introduces a multiprocessing system);

a local memory system executing a protocol to share data with at least one other processor unit (Chapter 2, page 13, section 2.1);

a conflicts resolution circuit executing a hardware program to resolve conflicts between different processor units;

a lock elision circuit executing a hardware program to:

(i) detect the start of execution by the processor of a critical section of a program subject to a lock (See 3.9.1.1 and page 51, lines 20-32);

(ii) speculatively execute the critical section without acquiring the lock (Section 3.2, page 50, line 32 - page 51, line 25 and Fig. 3-5);

(iii) when a conflict for data of the critical section is detected, refer the conflict to the conflict resolution circuit, where the conflict is indicated by a request by another processor unit for data in the critical section owned by the processor unit (Chapter 4, pages 100, lines 25-30, and page 101, lines 1-4); and

(iv) when no conflict for data of the critical section is detected, commit the execution of the critical section. See page 94, lines 9-14.

Response to Arguments

Applicant's arguments filed 6/12/2006 have been fully considered but they are not persuasive. The date that the doctoral thesis of Ravi Rajwar was first available to the public through the University Microfilm, Inc. asserted by the Applicant is noted, however this document would then be a 102(a) reference.

The examiner has included the dissertation with additional documentation on the publication date.

Conclusion

This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2189

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

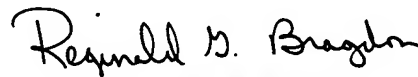
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thanh Vo
Patent Examiner
Art Unit 2189
6/26/2006



REGINALD G. BRAGDON
PATENT EXAMINER

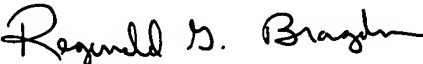
37 CFR 1.105 – Requirement for Information

Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

In response to this requirement, please indicate if the doctoral thesis titled "Speculation-based techniques for transactional lock-free execution o lock-based programs" authored by Ravi Rajwar has be indexed, cataloged and shelved in University of Wisconsin-Madison Library. If so, please provide the date that the doctoral thesis indicated above has been shelved in the university library.

The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained may be accepted as a complete reply to the requirement for that item.

The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.


REMOND G. DRACDON
PATENT EXAMINER